IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **RUAT ET AL.**	
Serial No. **10/824,932**	Examiner: **J. DSOUZA**
Filing Date: **APRIL 15, 2004**	Art Unit: **2611**
Confirmation No. **7552**	Attorney Docket No. **01RO12854443**
For: **ASYNCHRONOUS RECEIVER OF THE UART-TYPE WITH TWO OPERATING MODES**	

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite $540.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484.**

(1) Real Party in Interest

The real party in interest is STMicroelectronics SA, assignee of the present application as recorded at reel 1558, frame 83.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 1-6, 8-15 and 17-23 are rejected in the application, all of which being appealed herein. Claims 7, 16 and 24 have been cancelled.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

The present invention, as recited in independent Claim 1, is directed to an asynchronous frame receiver **UART1** comprising an input **RPD** to receive asynchronous frames comprising standard characters **SYNC/CH1/CH2-CHN**, and a header comprising a break character **BRK** with a data bit length greater than a data bit length of the standard characters. See page 2, paragraph 5; page 9, paragraph 37 through page 10, paragraph 38; and FIGS. 1 and 5 of the present application.

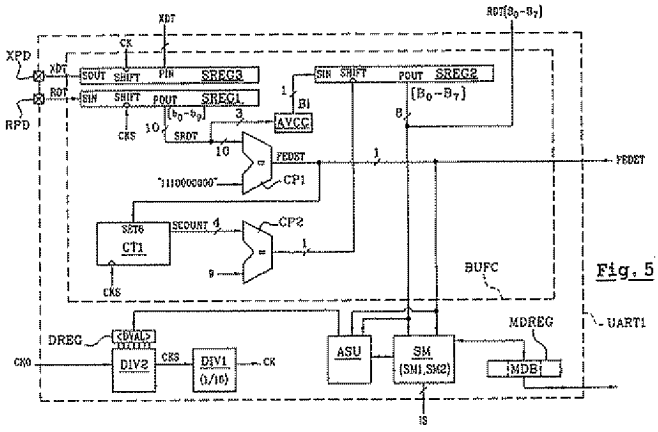

Fig. 5

FIG. 5 of the Present Application

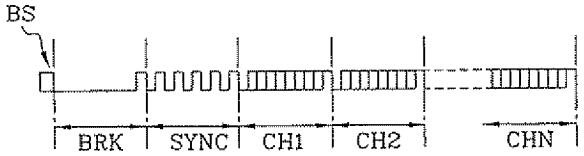

FIG. 1 of the Present Application

A first state machine **SM1** is configured as a break character detection unit to detect the break character, and a second state machine **SM2** is configured as a standard character processing unit to detect the standard characters. See page 6, paragraph 25 through page 7, paragraph 30; page 7, paragraph 31 through page 8, paragraph 32 and FIGS. 2 and 3 of the present application.

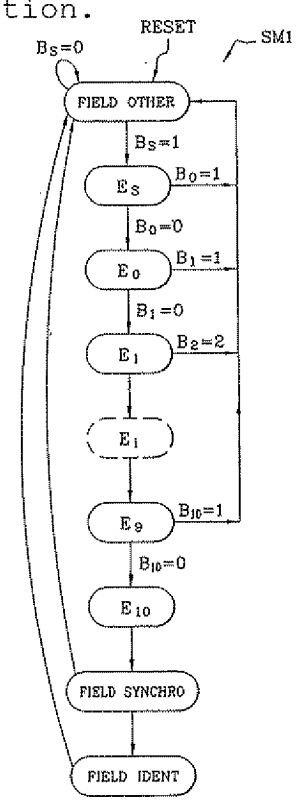

FIG. 2 of the Present Application

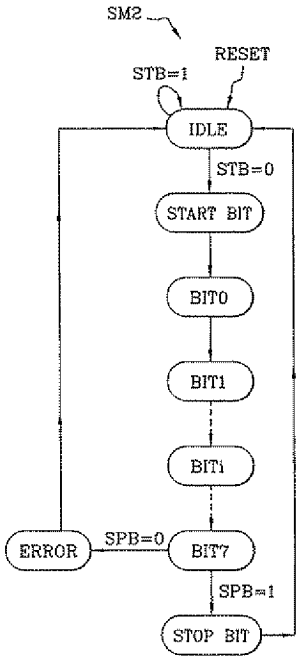

FIG. 3 of the Present Application

The first and second state machines **SM1**, **SM2** may be further configured so that in a first operating mode only the standard character processing unit is to operate, and in a second operating mode both the first and second state machines are to operate, with the break character detection unit to activate the standard character processing unit after the character break has been detected. See page 8, paragraph 33 of the present application.

An advantage of the claimed invention is that the first and second state machines **SM1**, **SM2** may be used to provide two operating modes in an asynchronous frame receiver **UART1**. For example, the first operating mode may be a conventional operating mode in which only the second state machine **SM2** is active. The second operating mode may be an operating mode dedicated to protocols of the LIN type, providing a break character BRK in a frame beginning. In the second operating mode, both state machines may be used in which the first state machine **SM1** activates the second state machine **SM2** after a break character **BRK** has been detected.

Independent Claim 10 is similar to independent Claim 1, and is directed to a microcontroller **MC** comprising a universal asynchronous receiver transceiver (UART). See page 13, paragraph 46, and FIG. 7. The UART comprises an input **RPD** to receive asynchronous frames comprising standard characters **SYNC/CH1/CH2-CHN**, and a header comprising a break character **BRK** with a data bit length greater than a data bit length of the standard characters. See page 2, paragraph 5; page 9, paragraph 37 through page 10, paragraph 38; and FIGS. 1 and 5 (reproduced above) of the present application.

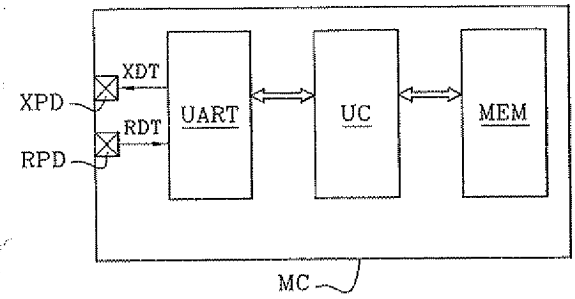

FIG. 7 of the Present Application

A first state machine **SM1** is configured as a break character detection unit to detect the break character. A second state machine **SM2** is configured as a standard character processing unit to detect the standard characters. See page 6, paragraph 25 through page 7, paragraph 30; page 7, paragraph 31 through page 8, paragraph 32 and FIGS. 2 and 3 (reproduced above) of the present application.

The first and second state machines **SM1**, **SM2** are further configured so that in a first operating mode only the standard character processing unit is to operate, and in a second operating mode both the first and second state machines are to operate. The break character detection unit activates the standard character processing unit after the character break has been detected. A processor **UC** is connected to the UART. See page 8, paragraph 33 of the present application.

Independent Claim 18 is similar to independent Claim 1, and is directed to method for processing asynchronous frames in an asynchronous frame receiver **UART**. The method comprises receiving as input by the asynchronous frame receiver **UART** the asynchronous frames comprising standard characters **SYNC/CH1/CH2-CHN**, and a header comprising a break character **BRK** with a data bit length greater than a data bit length of the standard characters. See page 2, paragraph 5; page 9, paragraph 37 through page 10, paragraph 38; and FIGS. 1 and 5 (reproduced

above) of the present application.

The break character is detected in the asynchronous frames using a first state machine **SM1** configured as a break character detection unit. A second state machine **SM2** configured as a standard character processing unit is activated based upon the break character detection unit detecting the break character. See page 6, paragraph 25 through page 7, paragraph 30; page 7, paragraph 31 through page 8, paragraph 32 and FIGS. 2 and 3 (reproduced above) of the present application.

The first and second state machines **SM1**, **SM2** are further configured so that in a first operating mode only the standard character processing unit is to operate, and in a second operating mode both the first and second state machines are to operate. The break character detection unit activates the standard character processing unit after the character break has been detected. See page 8, paragraph 33 of the present application.

(6) Grounds of Rejection to be Reviewed On Appeal

Claims 1-6, 8-15 and 17-23 stand rejected under the Gulick et al. patent in view of the Appellants' Admitted Prior Art, in view of the Sexton et al. patent, and in further view of the Hong et al. patent.

(7) Argument

I. Independent Claims 1, 10 and 18 Are Patentable

The Examiner rejected independent Claims 1, 10 and 18 over the Gulick et al. patent in view of the Appellants' Admitted Prior Art, in view of the Sexton et al. patent, and in further view of the Hong et al. patent.

The Examiner cited Gulick et al. as disclosing in FIG. 21 an asynchronous frame receiver comprising a break character detection unit **412** for detecting the break character. The Examiner has taken the position that Gulick et al. also discloses a standard character processing unit for detecting standard characters.

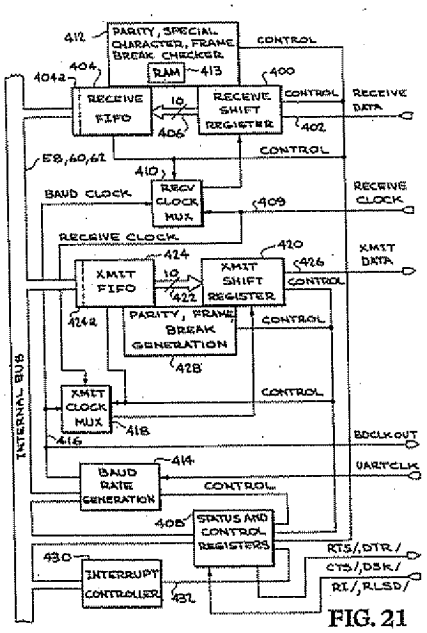

FIG. 21

FIG. 21 of Gulick et al.

As correctly noted by the Examiner, Gulick et al. fails to disclose an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters. The Examiner referenced paragraph 5 and FIG. 1 in the specification (Appellants' Admitted Prior Art as reproduced above) as disclosing a header comprising break and

standard characters.

The Examiner cited Sexton et al. as disclosing a header comprising a break character with a data bit length greater than a data bit length of the standard characters (column 3, lines 27-31). The Examiner correctly noted that Gulick et al. fails to disclose a break character detection unit comprising a first state machine, and wherein the standard character processing unit comprises a second state machine.

The Examiner cited Hong et al. as disclosing in FIG. 22 a state machine comprising a break character detection unit **198** and a standard character processing unit **202** (column 38, lines 1-41). As correctly noted by the Examiner, Hong et al. discloses that units **198, 202** are in a single state machine instead of separate state machines as in the claimed invention, but the Examiner references MPEP 2144.04 which states that separating elements to obtain the same function is not considered patentable, particularly if no new and unexpected result is produced.

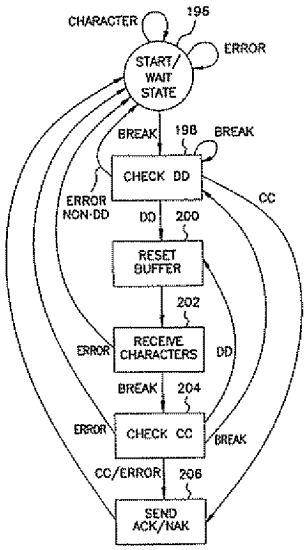

FIG. 22 of Hong et al.

The Appellants submit that new and unexpected results are obtained by having two separate state machines. Since the first state machine is configured to detect the break character within the header, it ensures a complete detection of the frame header before activating the second state machine for detecting the standard characters (when in the second operating mode). Reference is directed to paragraph 34 in the Appellants' specification. Another advantage is as disclosed in paragraph 45 in the Appellants' specification, as reproduced below:

> "Furthermore, according to an optional but advantageous aspect of the present invention, the circuit **UART1** further comprises a register **MDREG** in which a mode bit **MDB** accessible for reading and for writing from the outside environment is stored. When the mode bit has a first value, the circuit **UART1** operates as a conventional **UART** circuit, and state machine **SM1** is deactivated, as well as consequently the self synchronization unit **ASU**. When the mode bit has a second value, the two state machines **SM1**, **SM2** are operational and the circuit **UART1** can process complex frames such as for example **LIN** frames." (Emphasis added).

With the single state machine in Hong et al. operating as both a break character detection unit **198** and a standard character processing unit **202**, there is the potential that the break character detection unit **198** begins operation before the standard character processing unit **202** detects a frame header. In sharp contrast, for the second operating mode of the first and second state machines in the claimed invention, the second state machine (i.e., break character detection unit) activates the first state machine (i.e., standard character processing unit) after the character break has been detected. This is not always

possible with Hong et al.

Other advantages of the separate state machines are that different operating modes are supported. The first operating mode may be a conventional operating mode (in which only the second state machine is active), and the second operating mode may be an operating mode dedicated to protocols of the LIN type, for example, providing a break character **BRK** in a frame beginning. In the second operating mode, both state machines may be used in which the first state machine activates the second state machine after a character **BRK** has been detected.

The claims in the present invention recite that the asynchronous frames comprise standard characters, and a header comprises a break character **BRK** with a data bit length greater than a data bit length of the standard characters. The Examiner is using a three-way rejection to provide this feature of the claimed invention.

As noted above, the Examiner cited Gulick et al. as disclosing an asynchronous frame receiver comprising a break character detection unit **412** (FIG. 21, reproduced above) for detecting the break character. The Examiner has taken the position that Gulick et al. also discloses a standard character processing unit for detecting standard characters. As correctly noted by the Examiner, Gulick et al. fails to disclose an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters. The Examiner referenced paragraph 5 and FIG. 1 (reproduced above) in the specification (Appellants' Admitted Prior Art) as disclosing a header comprising break and standard characters. The Examiner cited Sexton et al. as disclosing a header comprising a break

character with a data bit length greater than a data bit length of the standard characters (column 3, lines 27-31).

The Appellants submit that is would not have been obvious to selectively combine the prior art references as suggested by the Examiner to produce this feature of the claimed invention. This is particularly so since the Sexton et al. patent fails to disclose that the controllers are operating as asynchronous frame receivers. Instead, the controllers in Sexton et al. communicate with each other via a common bus under the control of a master controller.

Accordingly, it is submitted that independent Claim 1 is patentable over the Gulick et al. patent in view of the Appellants' Admitted Prior Art, and further in view of the Hong et al. patent. Independent Claims 10 and 18 are similar to independent Claim 1. Therefore, it is submitted that these claims are also patentable over the Gulick et al. patent in view of the Appellants' Admitted Prior Art, and further in view of the Hong et al. patent.

In view of the patentability of independent Claims 1, 10 and 18, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

II. Conclusion

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision by the Examiner.

Respectfully submitted,

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APPENDIX A - CLAIMS ON APPEAL FOR U.S. PATENT APPLICATION SERIAL NO. 10/824,932

1. (Previously Presented) An asynchronous frame receiver comprising:

an input to receive asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

a first state machine configured as a break character detection unit to detect the break character;

a second state machine configured as a standard character processing unit to detect the standard characters; and

said first and second state machines being further configured so that

in a first operating mode only said standard character processing unit is to operate, and

in a second operating mode both said first and second state machines are to operate, with said break character detection unit to activate said standard character processing unit after the character break has been detected.

2. (Original) An asynchronous frame receiver according to Claim 1, further comprising a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit.

3. (Original) An asynchronous frame receiver according to Claim 1, wherein said break character detection unit detects a break character formed of bits having a same value.

4. (Original) An asynchronous frame receiver according Claim 1, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

5. (Original) An asynchronous frame receiver according to Claim 4, further comprising a self-synchronization circuit for synchronizing a local clock signal of the receiver with a reference clock signal in the synchronization character.

6. (Original) An asynchronous frame receiver according to Claim 5, wherein said self-synchronization circuit is activated by said break character detection unit.

Claim 7 (Cancelled).

8. (Original) An asynchronous frame receiver according to Claim 2, wherein said selection circuit comprises a register for storing a mode bit.

9. (Original) An asynchronous frame receiver according to Claim 1, further comprising a substrate, and wherein said break character detection unit and said standard character processing unit are on said substrate so that the receiver comprises an integrated circuit.

10. (Previously Presented) A microcontroller comprising:

a universal asynchronous receiver transceiver (UART) comprising

an input to receive asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters,

a first state machine configured as a break character detection unit to detect the break character,

a second state machine configured as a standard character processing unit to detect the standard characters, and

said first and second state machines being further configured so that

in a first operating mode only said standard character processing unit is to operate, and

in a second operating mode both said first and second state machines are to operate, with said break character detection unit to activate said standard character processing unit after the character break has been detected; and

a processor connected to said UART.

11. (Original) A microcontroller according to Claim 10, wherein said UART further comprises a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in

which said break character detection unit is active and controls said standard character processing unit.

12. (Original) A microcontroller according to Claim 10, wherein said break character detection unit detects a break character formed of bits having a same value.

13. (Original) A microcontroller according Claim 10, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

14. (Original) A microcontroller according to Claim 13, wherein said UART further comprises a self-synchronization circuit for synchronizing a local clock signal of said UART receiver with a reference clock signal in the synchronization character.

15. (Original) A microcontroller according to Claim 14, wherein said self-synchronization circuit is activated by said break character detection unit.

Claim 16 (Cancelled).

17. (Original) A microcontroller according to Claim 11, wherein said selection circuit comprises a register for storing a mode bit.

18. (Previously Presented) A method for processing asynchronous frames in an asynchronous frame receiver, the method comprising:

receiving as input by the asynchronous frame receiver the asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

detecting the break character in the asynchronous frames using a first state machine configured as a break character detection unit;

activating a second state machine configured as a standard character processing unit based upon the break character detection unit detecting the break character; and

the first and second state machines being further configured so that

in a first operating mode only the standard character processing unit is to operate, and

in a second operating mode both the first and second state machines are to operate, with the break character detection unit to activate the standard character processing unit after the character break has been detected.

19. (Original) A method according to Claim 18, wherein the asynchronous frame receiver comprises a selection circuit for selecting a first operating mode in which the break character detection unit is deactivated, or a second operating mode in which the break character detection unit is active and controls the standard character processing unit.

20. (Original) A method according to Claim 18, wherein the break character detection unit detects a break character formed of bits having a same value.

21. (Original) A method according Claim 18, wherein the asynchronous frames comprise a synchronization character, and wherein the break character detection unit detects the synchronization character.

22. (Original) A method according to Claim 21, wherein the asynchronous frame receiver further comprises a self-synchronization circuit for synchronizing a local clock signal of the asynchronous frame receiver with a reference clock signal in the synchronization character.

23. (Original) A method according to Claim 22, wherein the self-synchronization circuit is activated by the break character detection unit.

Claim 24 (Cancelled).

APPENDIX B – EVIDENCE APPENDIX

PURSUANT TO 37 C.F.R. § 41.37(c)(1)(ix)

None.

APPENDIX C – RELATED PROCEEDINGS APPENDIX PURSUANT TO 37 C.F.R. § 41.37(c)(1)(x)

None.